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SUMMARY

A concept for performing radiometric correction of multispectral image data onboard a spacecraft at very high data rates is presented and demonstrated. This concept utilizes a lookup table approach, implemented in hardware, to convert the raw sensor data into the desired corrected output data. The digital lookup table memory is interfaced to a microprocessor to allow the data correction function to be completely programmable. Sensor data can be processed with this approach at rates equal to the access time of the lookup table memory. This concept offers flexible high speed data processing for a wide range of applications and will benefit from the continuing improvements in performance of digital memories.

INTRODUCTION

Because of the large quantities of data space-acquired multispectral image which make up an image, the process of information extraction is both time consuming and expensive. Onboard data processing is one of the ideas under investigation to simplify the processing requirements. Different opinions exist on the benefits of onboard processing, since many experimenters would like to process image data with their own algorithms. However, researchers accept onboard radiometric correction more readily than other onboard processing functions. The removal of variations in sensor gain and offset is the initial step performed in virtually all image processing algorithms. Performing this function onboard the spacecraft would allow users to receive preprocessed data directly and would offer potential processing cost savings. The cost of the radiometric correction can be included in the cost of the imaging system. The correction of gain and offset variations is also reversible for those algorithms in which the original unprocessed data is desired. Finally, this single technology development can be applied to many instruments over a long period of time.

This paper describes a technique for performing radiometric correction onboard a spacecraft using state-of-the-art digital techniques. This approach utilizes the lookup table concept used in many computer software routines; however, the concept is implemented in hardware to achieve the high operational speed necessary for real-time onboard processing. The concept will allow the radiometric correction to be programmable to accommodate temperature changes or long term changes in sensor characteristics. The concept will also exploit continuing improvements in memory technology which will reduce cost and improve performance of the onboard processing hardware. Finally, this concept can also be adapted to many other signal processing applications in which high speed computation of single valued functions is required.

LOOKUP TABLE APPROACH

The lookup table (LUT) concept is nothing more than reading information from a table. In a typical software application, input data would be used to compute an address in memory from which the desired output value would be read from a lookup table. This method requires several machine cycles of the computer and hence cannot be used for real-time processing at high data rates. The approach described here is to use special purpose hardware without a central processor to actually apply the gain and offset corrections. The primary speed limitation in this configuration is the memory cycle time, which is typically several times faster than the execution of single machine instruction.

The hardware lookup table approach to high speed processing is illustrated in figure 1. The system is generally partitioned into two sections, the high speed lookup table memory and the control circuitry which includes a microprocessor. Correction data to be stored in the lookup table can be computed by the microprocessor or computed externally and transferred to the microprocessor system memory through a direct memory access (DMA) channel. The desired output values are loaded into the lookup table memory through the memory address bus and data bus. The lookup table memory can be selected to accommodate the work length of the sensor data. Once the memory has been loaded, the microprocessor outputs control information to configure the data and address buses of the lookup table memory to process the sensor data. A sensor data value is applied to the address bus to select a specific memory location. The desired output value for that input sensor data value is then read from that memory location and placed on the output data bus for the next processing function or for transmission to the ground.

A limitation of this approach is that the lookup table memory cannot be used to process data while table values are being loaded. For certain high speed data processing applications, this down time is very undesirable. There are two configurations which minimize this down time.

In the first configuration, the lockup table memory is loaded as fast as possible through a DMA channel. If a single DMA channel is used to read values out of the system memory, separate hardware must be used to generate the addresses, timing, and control to write the data into the lookup table memory.

The second approach is conceptually simple and easy to implement. It involves switching between redundant lookup table memories in a ping-pong configuration. One memory can be loaded with new correction data by the microprocessor while the other is processing sensor data. Data can be moved to the lookup table memory under software control at relatively slow rates using normal memory-to-memory transfer instructions. Upon completion of the loading process, the microprocessor can enable the second memory using the bus control switches. The transition from one lookup table memory to the other can be accomplished with sufficient speed to lose at most a single data value; more likely no data at all would be lost. This additional flexibility, reliability, and minimization of the down time for signal processing can be achieved with the addition of only the second lookup table memory and switches and a slight increase in software complexity.

The hardware lookup table concept has another significant advantage in addition to the very high speed data processing capability. While the lookup table memory is configured to process data, the microprocessor is totally free to perform other software tasks. Hence the system design engineer now has a new opportunity to trade off microprocessor speed, complexity, and cost, while maintaining a high level of signal processing performance.

APPLICATION TO RADIOMETRIC CORRECTION

Typical radiometric correction of sensor data includes the application of gain and offset corrections to produce output sensor values which closely represent the input radiance to the sensor. In cases where the sensor output transfer function is not linear, several gain adjustments may be required to linearize the sensor output. Implementation of a piecewise linear fit for each sensor requires considerable hardware complexity and results in potential losses in accuracy depending upon the degree of nonlinearity of the detector response. This problem is significantly reduced with the use of the lookup table concept since each input value is mapped directly to an output value, so that nonlinear processing functions can be implemented.

For 8-bit input data, there are 256 possible table values for the output function. Hence each kilobyte of random access memory (RAM) would support four sensor elements. Data from a 1000-element sensor array could be processed with 256 kilobytes of memory. The selection of the appropriate mapping function for each photosensor element could be accomplished as shown in figure 2. Using the output of a counter to provide the most significant bits of the RAM address allows the correct 256-byte block of memory to be selected for each photosensor. The clock pulses which are used to shift the sensor data can generate the clock input to the counter. Line synchronization pulses from the photosensor can be used to reset the counter.

In cases where many detector response curves can be represented by the same output values, the configuration shown in figure 3 can reduce the required lookup table memory size. A secondary RAM is used to map all of the counter values or sensor elements which have the same desired output values to the same 256-byte block of memory. In this configuration the size of the memory can also be traded off as a function of the required accuracy, since groups of almost identical mapping functions could be represented by a single function (256-byte memory block).

DESIGN OF TEST LOOKUP TABLE

A lookup table memory system was designed to demonstrate the feasibility of the concept and evaluate its potential performance. A Motorola M6800 microprocessor[1] and an 8 × 1024 bit static RAM were used in the test system as shown

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[1]Use of the manufacturer's name does not constitute endorsement, either expressed or implied, by NASA.

in figure 4. Since 8-bit sensor data were assumed, the 1024-byte lookup table memory allows four separate tables of corrected data with 256 bytes each. Bidirectional bus switches, under the control of a Motorola peripheral interface adapter (PIA), connect the bus and control lines of the LUT memory in either the microprocessor or the sensor processiong mode.

Mode selection is performed by a software output routine which sends a mode command via a PIA bit to the control input of the bus switches. In the microprocessor system mode, the LUT memory is part of the system memory map. Software is executed to compute the desired output values and load them into the LUT. In the sensor processing mode, the mode control bit is cleared through the PIA to removing the LUT from the microprocessor system memory. Two additional PIA bits are used to select one of the four blocks of 256 bytes within the LUT memory containing the desired corrected values.

Eight-bit sensor data are applied to the memory address bus through the bus switches. A digital latch is used to hold valid data on the memory data bus to allow simpler synchronization of the output data with subsequent processing functions.

Control logic ensures that the data clock pulses can be properly synchronized with the sensor data to allow memory operation at maximum specified rates. When the system enters the sensor processing mode, the control logic sets the memory read/write (R/W) signal high, so that the LUT memory is in the read mode for the duration of the data output cycle. Figure 5 shows the signal timing diagram for the LUT memory. Timing parameters indicated in the figure are defined in the appendix. The memory select and latch enable commands are generated within the control logic as a function of the rising edge of the sensor data clock pulse. The rising edge of the data clock pulse is coincident with a change in the digital sensor data (lines 1 and 2 of fig. 5) at the address input of the system. The rising edge of the clock pulse for the initial input data byte causes the control logic to select the LUT memory (line 3 of fig. 5). The memory will remain enabled until the mode input to the logic indicates a return to the microprocessor mode. After the input data byte is resident on the memory address lines for a duration equal to the memory access time t_a, the valid output data value appears on the memory output data lines (line 5 of fig. 5). This output data value is the corrected version of the sensor data value that resides on the memory address lines.

Since the output data value remains valid only for the time interval t_v, a digital latch is employed at the memory data lines to hold the data value until the next byte is ready for output (line 7 of fig. 5). The control generator of the test system provides an enable pulse to the latch during t_v that allows the latched output to follow the input when the pulse is high and latches the input to the output when it becomes low (line 6 of fig. 5). Generation of this latch enable pulse is accomplished by two one-shot circuits within the control generator. The first one-shot circuit uses the rising edge of the data clock pulse to generate a memory access timing pulse (line 4 of fig. 5). This timing pulse remains low for the specified access time t_a of the memory; therefore, it rising edge denotes the presence of valid data at the memory output data lines and the latch input. When this rising edge appears at the input of a second one-shot circuit, the latch enable command

is generated. The output data value is maintained at the latched system output for a time interval equal to the period of the data clock.

PERFORMANCE EVALUATION

The test lookup table system was evaluated to determine the maximum operational speed for processing sensor data. A lookup table memory with an access time t_a of 200 nanoseconds allowed a maximum data processing rate of 5 megabytes per second. The control logic was developed to allow operation over a wide range of clock frequencies to accommodate a variety of system applications. Several output mapping functions were developed on the M6800 microprocessor to demonstrate the processing flexibility of the lookup table concept. In the test configuration, a binary counter was used as a digital data source to simulate sensor data. Digital-to-analog (D/A) converters were used to display the input sensor data and the processed output data on an oscilloscope.

The test lookup table system operated successfully over input data rates from 1 hertz to 5 megahertz; thus data could be processed at speeds equal to the memory access time. Figure 6 illustrates two output mapping functions and the linear input ramp generated by the digital counter. The output data shown in figure 6 were processed at the 1.5 megahertz sample rate and illustrate that complex nonlinear mapping functions can be easily implemented. The bus switches which were utilized for the test system operate with switching times of 25 nanoseconds. These high speed switches allow sensor data to be switched to different memory blocks containing different mapping functions without loss of processed data. These test results indicate that higher speed memories, with 55-nanosecond access time, for example, could be used to process data at even higher speeds.

The process of latching valid output data from the lookup table memory becomes more complex as the sensor data rate inceases. When the frequency of the sensor data approaches the rated operating frequency of the lookup table memory ($1/t_a$), the valid output data time interval t_v is reduced to the hold time t_h characteristic of the memory. This hold time (line 5 of fig. 5) is the interval that a memory output data value remains valid after an address change. To ensure that data are continually valid at the system output, the latch enable pulse width t_w, must not exceed t_h. For high data rate applications, edge-triggered D flip-flops could be used to provide the latching function. Propagation delays in the system bus switches have a significant effect on data latching when high speed memories are employed to accommodate high input data rates. These propagation delays cause a shift in the output data relative to the access timing and latch enable functions. As a result, the latch could be enabled before the data value is valid at its input. To prevent such a system malfunction, the data clock should be routed through a bus switch to the control generator input, and similarly, the latch enable should be delayed by a bus switch before arriving at the latch. This configuration synchronizes the latch enable command with the data flow and ensures proper system operation in high frequency data processing applications.

CONCLUDING REMARKS

A concept for onboard signal processing of multispectral image data to remove variations in photosensor characteristics has been presented. This concept provides high speed flexible signal processing by implementing a software lookup table approach in hardware. For each sensor data value, the corrected output value desired by the user is stored in the lookup table memory. Sensor data are applied to the address lines of the lookup table memory and the desired processed output data value is read from the memory.

A test lookup table memory was implemented and successful operation was demonstrated. A data processing throughput rate of 5 megahertz was demonstrated; this rate was limited by the access time of the lookup table memory. Improved signal processing performance could be obtained by utilizing higher speed memory devices. A conceptually simple system configuration was demonstrated which allows microprocessor interface to compute and transfer the desired output values into the lookup table. During normal processing of sensor data, the lookup table is free from the microprocessor data and address buses; therefore the microprocessor can perform additonal tasks unrelated to the signal processing. A ping-pong architecture was described which allows signal processing to continue as new output values are loaded into an additional lookup table memory.

This signal processing concept offers several advantages for future onboard applications. Implementation of the concept will become more cost effective and beneficial as the development of high speed memory devices continues as a major technology thrust. Since the architecture is easily interfaced to a microprocessor, is completely programmable, and operates over wide bandwidth ranges, the concept will apply to many signal processing applications requiring complex computations and high processing speed.

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APPENDIX

TIMING PARAMETERS FOR THE TEST LOOKUP TABLE SYSTEM

The timing parameters indicated in figure 5 are defined as follows:

t_a memory access time, time interval between the application of an address on the memory address lines and the appearance of valid data on the memory output data lines

t_v valid data time, time interval in which data are valid on the memory data lines

t_h valid data hold time, time interval in which data remain valid after a change of address on the memory address lines

t_w latch enable pulse width

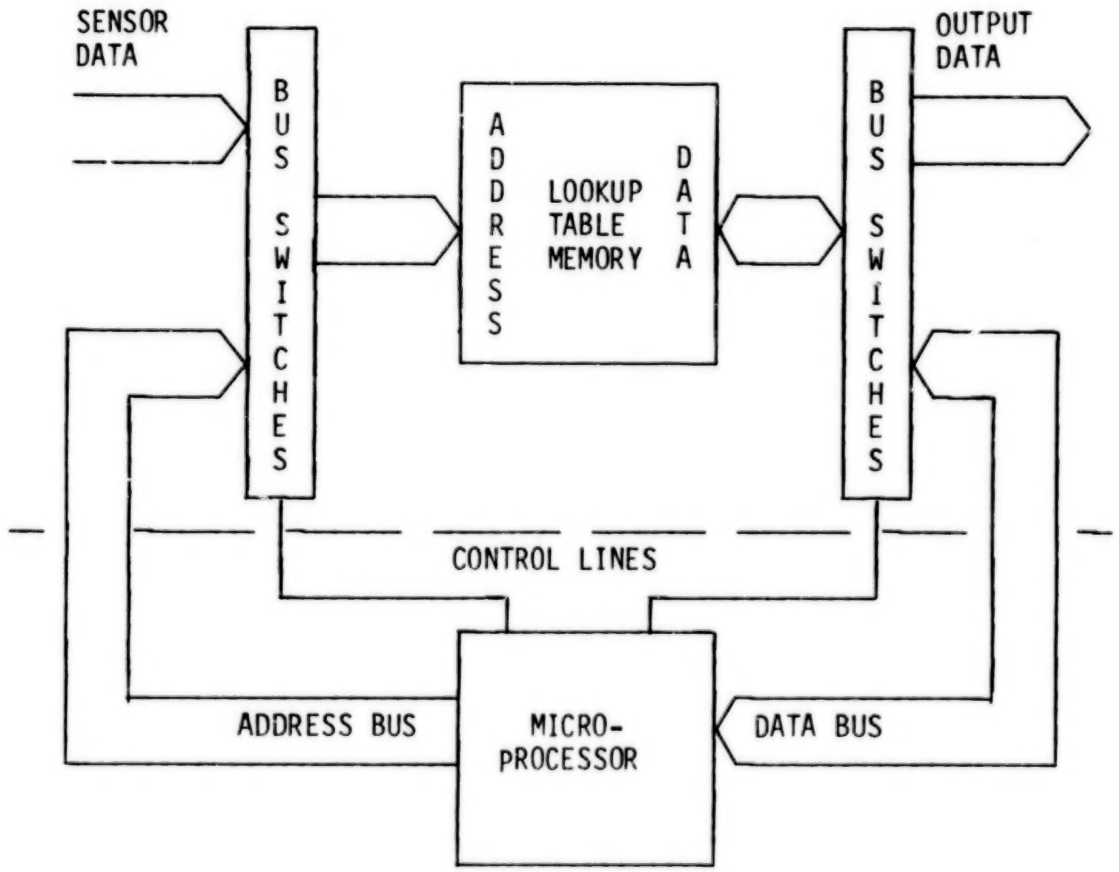


Figure 1.- Functional diagram of hardware lookup table.

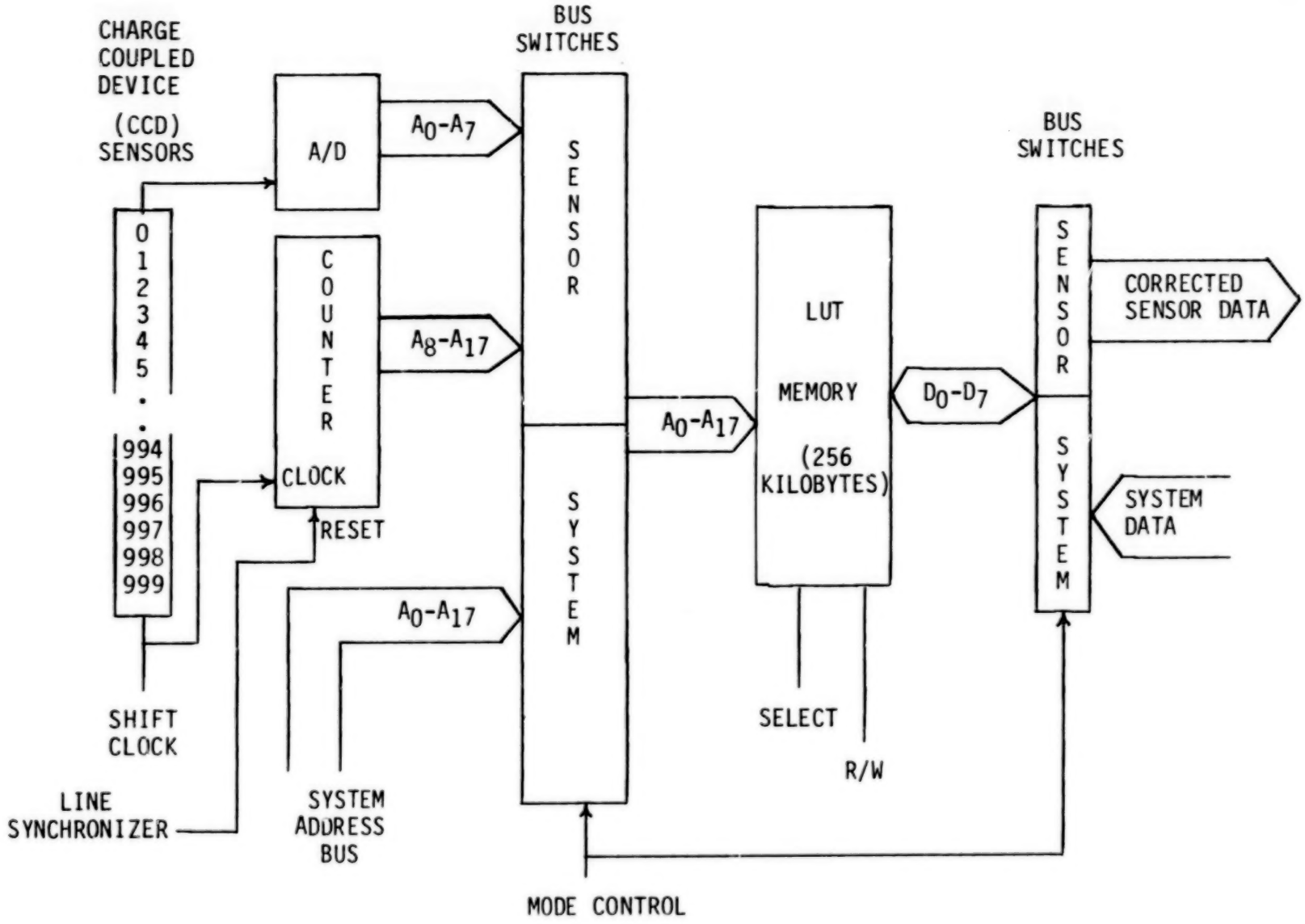


Figure 2.- Application of lookup table approach to radiometric correction for 1000-element sensor array.

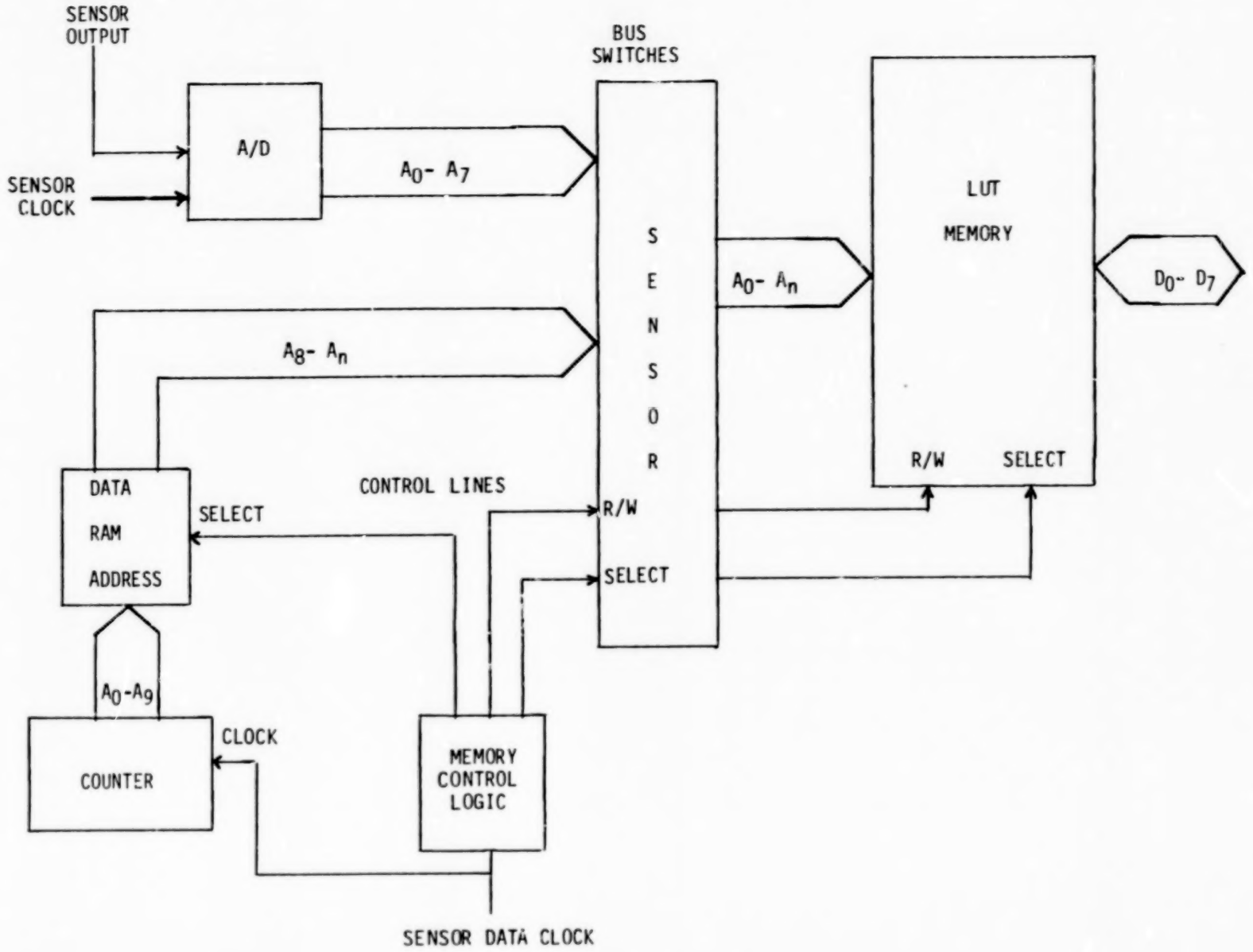


Figure 3.- Two-tiered RAM approach for reducing lookup table memory size.

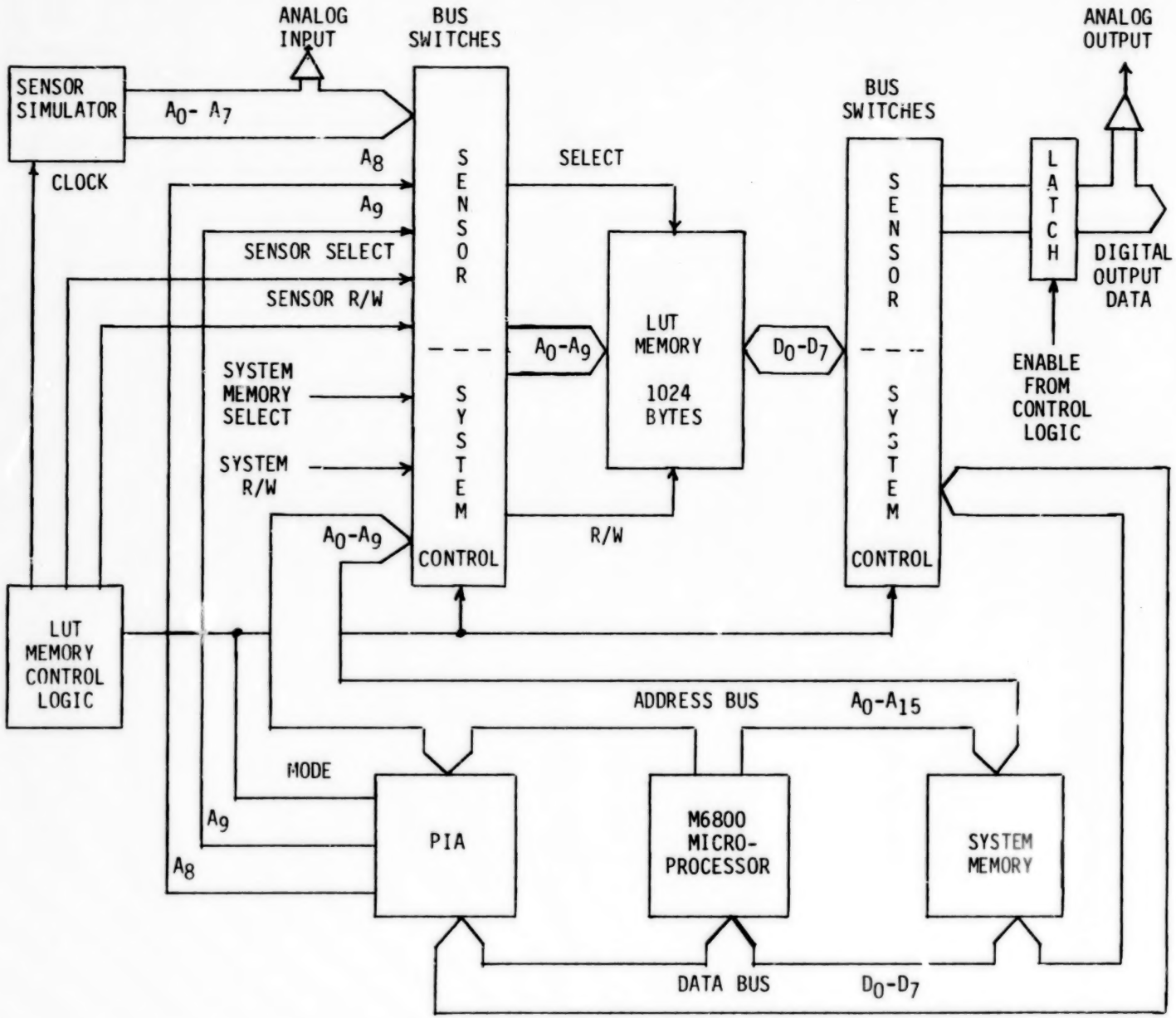


Figure 4.- Configuration of test lookup table system.

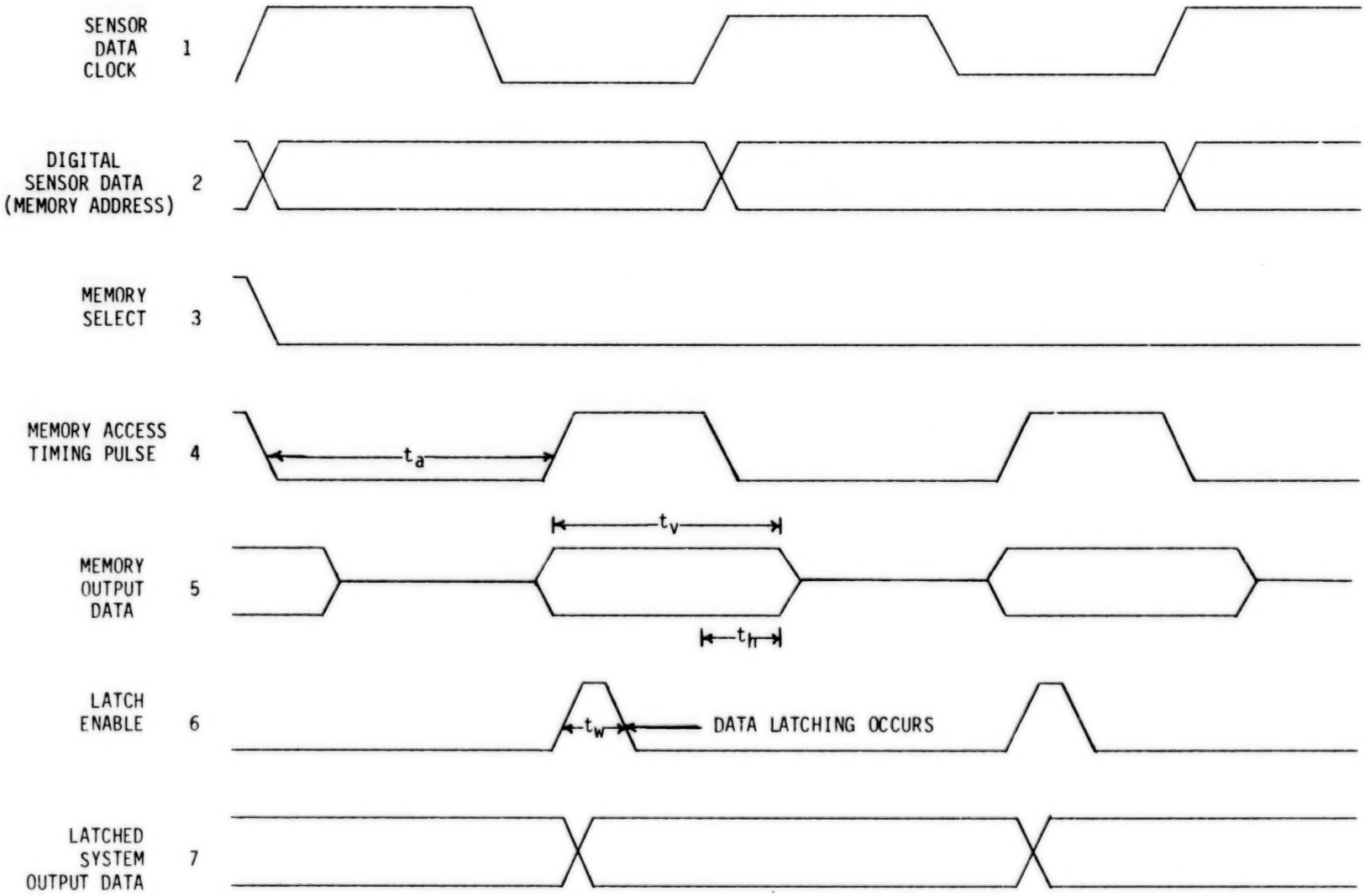
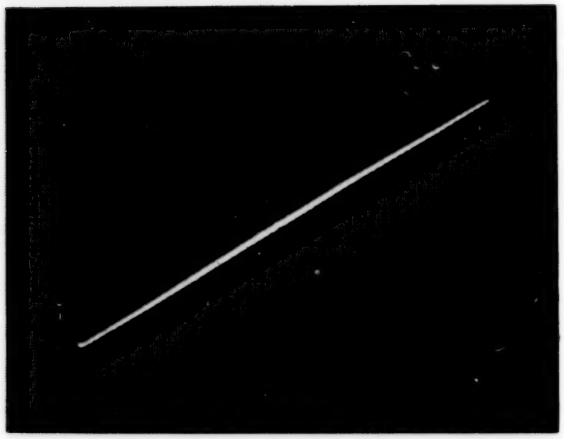
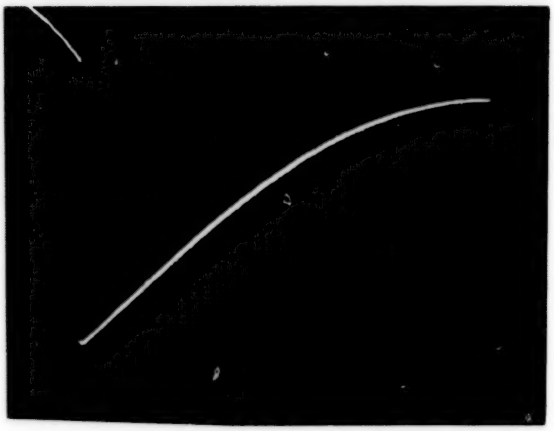


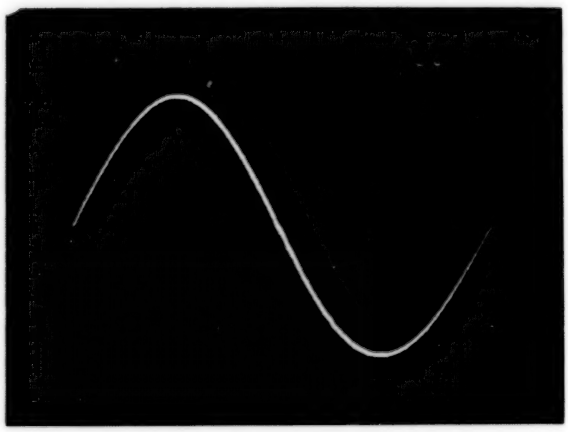
Figure 5.- Signal timing diagram for lookup table memory.



(a) Input ramp.



(b) F(X) = sin x/4.



(c) F(X) = sin x.

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Figure 6.- Analog representation of test system input signal and output mapping functions F(X).

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16. Abstract

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